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**Barth et al.**

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CPC ..... *G06F 13/161* (2013.01); *GIIC 5/066* (2013.01); *GIIC 7/10* (2013.01); *GIIC 7/1072* (2013.01); *GIIC 7/22* (2013.01); *GIIC 8/12* (2013.01)

(58) **Field of Classification Search**

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(73) Assignee: **Rambus Inc.****Reexamination Request:**

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(\*) Notice: This patent is subject to a terminal disclaimer.

**Related U.S. Application Data**

(60) Continuation of application No. 09/480,767, filed on Jan. 10, 2000, now Pat. No. 6,810,449, which is a continuation of application No. 08/979,402, filed on Nov. 26, 1997, now Pat. No. 6,122,688, which is a division of application No. 08/545,292, filed on Oct. 19, 1995, now Pat. No. 5,748,914.

(51) **Int. Cl.***G06F 13/16* (2006.01)*GIIC 7/22* (2006.01)*GIIC 8/00* (2006.01)*GIIC 7/10* (2006.01)*GIIC 8/12* (2006.01)(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 95/001,169, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

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(57)

**ABSTRACT**

A system and method for performing data transfers within a computer system is provided. The system includes a controller configured to dynamically adjust the interleave of the communications required to perform a series of data transfer operations to maximize utilization of the channel over which the communications are to be performed. The controller is able to vary the time interval between the transmission of control information that requests a data transfer and the performance of the data transfer by signaling the beginning of the data transfer with a strobe signal sent separate from the control information. The controller is able to defer the determination of how much data will be transferred in the operation by initiating the termination of a data transfer with a termination signal. The method provides a technique for distinguishing between identical control signals that are carried on the same line. The system includes a memory device with control circuitry that allows no more than one memory bank powered by any given power supply line to perform sense or precharge operations.

